

## FEATURES

The CPU unit of the ZAT-2000 MP control system (part of direct control level of ZAT-Plant Suite MP system).

**CPU Options:** The configuration table illustrates the capabilities of available CPUs. The 68060 processors operating at 50 MHz deliver up to 100 MIPs while the 68040 processors operating at 33 MHz give performances up to 35 MIPs.

**68EN360:** 25/33MHz – the ‘QUICC’ chip used in “companion mode” is tightly coupled to the CPU. Working as an I/O and system controller, it provides all the necessary interfaces, timers and clocks etc. In addition to the DRAM memory controller.

**Serial Channels:** Six are provided by the ‘QUICC’- Two SMC channels are ported to the front panel and the remaining four SCC channels may be optionally configured as shown.

**Ethernet Interface:** Two different piggybacks complete with all the associated control logic are available providing 10Base2 or 10BaseT interfaces.

**RS232 Serial Interfaces:** Two piggybacks are available with RJ45 connectors for MODEM compatible communications.

**DMA Channels:** 2 independent channels are provided by the ‘QUICC’ chip and can be used by applications requiring data transfer between CXC-modules, DRAM, FLASH memory, dual-ported SRAM. This memory can be configured with different memory options allowing tremendous flexibility when customising memory requirements for real-time applications.

**DRAM/FLASH:** This memory, complete with a 32 bit-wide access bus is placed on a piggy-back with addressing capability for up to two memory banks of 64 MByte each. On-board +5V FLASH memory provides the latest ROM technology allowing the user to take advantage of the onboard programming facility to produce low cost upgrades by simply overwriting existing stored data.

**SRAM:** This is dual-ported battery-backed (Goldcap) memory area with a 16 bit-wide access bus. Users of the IEC821bus and the onboard CPU both have access to this memory. The lower 8 kByte are reserved for the location monitor.

**EEPROM:** Although a 2 kbit EEPROM is provided on-board, 1 kbit has been pre-programmed with unit production data (boot info, Ethernet registration, etc.) leaving the remaining available space for user application code. A write protect jumper prevents accidental erasure.

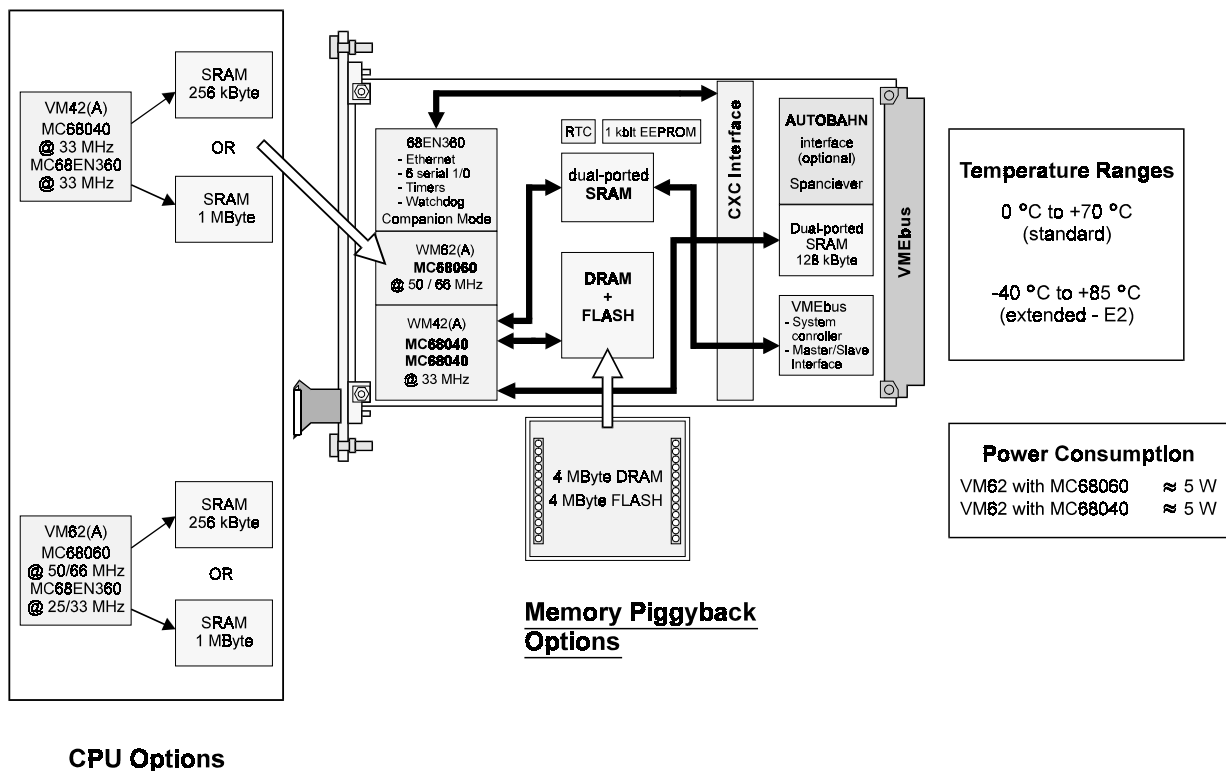
<i>Processor</i>	<i>Product</i>	<i>CPU</i>	<i>MMU</i>	<i>FPU</i>	<i>Supply</i>
<i>MC68040</i>	VM42(A)	❖	❖	❖	5V
<i>MC68EC060</i>	VM62(A)	❖	❖	❖	3,3V

## Specifications

<b>CPUs</b>	MC68060@ 50 MHz (3.3 V) MC68040@ 33 MHz
<b>Comms. Controller</b>	MC68EN360@ 25/33 MHz
<b>Memory</b> (piggyback module DM600)	4 MByte (32-bit access) DRAM 4 MByte (32-bit access) FLASH 1 MByte (16-bit wide) dual-ported SRAM with data retention via GOLDCAP 1 kbit serial EEPROM for applications
<b>Real-Time Clock</b>	V3021 3-wire serial interface (year, month, week, day, hour, min., sec.)
<b>Tick</b>	Built-in on MC68EN360 providing a programmable periodic interrupt
<b>Timer</b>	4x16, 2x32-bit resolution built-in timers on the MC68EN360
<b>Time-Out</b>	On-board BERR* time-out fixed at 8qs, software enable/disable
<b>Watchdog</b>	Enabled by software access integrated in on-board logic with front-panel LED
<b>Interrupts</b>	IRQ1*-IRQ7* interrupts, enable/disable; SYSFAIL* and ACFAIL* handlers
<b>System Autovectors</b>	Abort switch level 7 autovector ACFAIL* level 7 autovector TICK level 6 vector prog. SYSFAILS level 5 autovector Mailbox IRQ level 3 autovector
<b>Bus Request/ Arbitration Clock</b>	Single-level (BR3*), daisy-chain logic RWD (Release When Done) VME/CXC clock : 16Mhz CPU clock : 33 or 50 MHz Comms. Clock : 24 MHz
<b>System Controller</b>	SYSRES* (Removable from the IEC821bus by jumpers) SYSCLK* ACFAIL* SYSFAIL*
<b>Address Modifier</b>	Standard/User/Data : HEX 39/3A/3D/3E User Defined : HEX 10-17/18-1F short I/O : HEX 29/2D

<b>Slave Function</b>	Mailbox Interrupt dual-ported SRAM; up to 16 software selectable base addresses
<b>CXC</b>	DIN 41612 ©, 96pin, 3NMSI ports, DMA
<b>Interface</b>	
<b>IEC 821 Interface</b>	DIN 41612 ©, 96-pin P1 connector A24:D16/D8 master and slave
<b>Power Consumption</b>	VM62 / MC68060      ≈ 5 W @ 50 MHz VM42 / MC68040      ≈ 7 W @ 33 MHz
<b>Temperature</b>	0°C to +70°C (standard) -40°C to +85°C (extended)
<b>Humidity</b>	0 to 95% non-condensing
<b>Weight</b>	270 g (with 10Base T and memory piggybacks interface)
<b>Dimensions</b>	100 mm x 160 mm single-height 3U format
<b>Front Panel Functions</b>	3 LEDs:    red     : Halt yellow : Watchdog enabled green  : General purpose

**Block scheme of unit**



## Ordering Information

Product	Description	Order No.
DM 600	Memory Piggyback with 4 MByte DRAM and 4 MByte FLASH memory for VM42/62	11853
DM 602	Memory module with 1 MByte DRAM and 2 MByte FEPR0M for VSBC-32/860 VM42/62/642/662/162/172, IUC-32. Cannot be sold without CPU-BASE-Board.	17556
VM42-BASE	Same as order No. 12344 but with 1 MByte dual-ported SRAM	12345
VM42-BASE-E2	VMEbus CPU, 68040 33MHz, 68EN360 33MHz, 2*RS232, 1MB DP-SRAM, RTC, CXC Interface PEPbug. Extended temperature -40 to +85 °C. *E2 Memory must be ordered separately.	15818
VM62-BASE	VMEbus CPU, 68060 66MHz, 68EN360 33MHz, 2*RS232, 1024KB DP-SRAM, RTC, CXC Interface PEPbug. *Memory must be ordered separately. *SI piggyback must be ordered separately.	16625
VM62-BASE-E2	VMEbus CPU, 68060 50MHz, 68EN360 25MHz, 2*RS232, 1MB DP-SRAM, RTC, CXC Interface PEPbug. E2 (-40 to +85 °C). *Memory must be ordered separately. *SI piggyback must be ordered separately.	17665
10B2	10Base2 Thin Ethernet interface piggyback with RG58 coax. connector	9925
SI-10BT	Twisted pair (10BaseT) interface for use on the VM42/VM62, VSBC-32 or IUC-32. RJ45 connector cannot be sold without VM42-BASE or VM62-BASE or VSBC32x-BASE or IUC-32x-BASE. Shield connected with GND for CE qual.	15917
SI-10BT-E2	Twisted pair (10BaseT) interface for use on the VM42/VM62, VSBC-32 or IUC-32 in E2. RJ45 connector cannot be sold without VM42-BASE or VM62-BASE or VSBC32x-BASE or IUC-32x-BASE.	15819