

## FEATURES

The CPU unit of the ZAT-2000 MP control system (part of direct control level of ZAT-Plant Suite MP system).

**68(EN)360:** A 25/33 MHz full 32-bit CPU (CPU32 + core) with I/O and system controller providing all the necessary interfaces, timers and clocks etc. in addition to the DRAM memory controller.

**Serial Channels:** Six are provided by the 'QUICC'. Two SMC channels are ported to the front panel and the remaining four SCC channels may be optionally configured as shown.

Each VSBC-32 comes complete with 2 RS232 serial interfaces provided by the SMC1 and SMC2 channels of the QUICC controller ported to the lower half of the front panel. The SCC1 channel of the QUICC provides the interface to one of the available SI-x piggybacks. All other channels (SCC2, SCC3 and SCC4) of the QUICC are ported to the CXC interface except for the SI-PB232 piggyback which has additional control provided by the SCC4 channel.

**CXC-Interface:** The 96-pin interface allows other I/O possibilities to be realized by utilising PEP's plug-in cards with digital, analog, serial and SCSI interfaces. Fieldbus controllers complete the interface range.

**Ethernet Interface:** Three different SI piggybacks equipped with all the associated control logic are available for the 'EN' version providing 10Base2, 10Base5 or 10BaseT interfaces.

**RS232 Serial Interfaces:** Two SI piggybacks provide MODEM compatible RS232 communications.

**RS485 Fieldbus Interfaces:** This SI piggyback provides is a fully optoisolated RS485 interface piggyback with a 9-pin D-Sub connector.

**DMA Channels:** Two independent channels are provided by the 'QUICC' chip for use by applications requiring DMA transfer between VMEbus, CXC-modules, DRAM, FLASH memory and dual-ported SRAM.

**DRAM/FLASH:** This memory, complete with a 32 bit-wide access bus is placed on a piggyback with addressing capability for up to two memory banks of 64 MByte each. The on-board programmable FLASH memory allows the user to produce low-cost upgrades by overwriting existing stored data and may also be configured as a boot device.

**SRAM:** This is dual-ported battery-backed (Goldcap) memory area with a 16 bit-wide access bus. Users of the VMEbus and CPU both have access to this memory.

**EEPROM:** A 2 kbit EEPROM is provided on-board, 1 kbit has been pre-programmed with PEP production data leaving the remaining available space for user application code.

**Boot ROM/FLASH:** Two DIL sockets supporting up to 1 Mbyte of 16-bit ROM/FLASH memory are available for use as main memory or as a boot device if the FLASH appearing on the DM60x piggyback is not required.

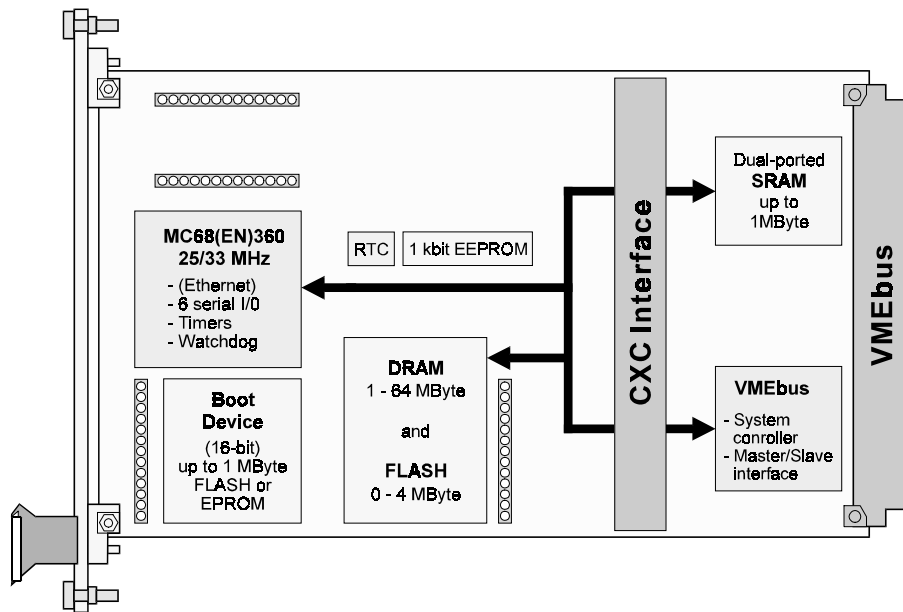
## Specifications

<b>CPUs</b>	MC68360 @ 25 MHz MC68EN360 @ 33 MHz
<b>Memory</b>	1/4/8/16/32/64 MByte (32-bit access) DRAM <sup>1</sup> 1/4 MByte (32-bit access) FLASH 256 kByte or 1 MByte (16-bit access) ROM or FLASH 256 kByte or 1 MByte dual-ported SRAM with data retention via GOLDCAP 2 kbit serial EEPROM for applications
<b>Real-Time Clock</b>	V3021 with year, month, week, day, hour, min., sec.)
<b>Tick</b>	Built-in on MC68EN360 providing a programmable periodic interrupt
<b>Timer</b>	4x16, 2x32-bit resolution built-in timers on the MC68(EN)360
<b>Time-Out</b>	On-board BERR* time-out fixed at 8 $\mu$ s, with software enable/disable
<b>Watchdog</b>	Enabled by software with front-panel LED; generates RESET
	All serial port baud-rate clocks may be configured individually by software
<b>Innterrupts</b>	VMEbus IRQ1*-IRQ7* interrupts, enable/disable; SYSFAIL* and ACFAIL* handlers
<b>System Controller</b>	Single level (BR3*), FAIR, RWD, Release When Done); Automatic First-Slot Detection VME and DP SRAM Read-Modify-Write cycle support
<b>Address Modifier</b>	A24 Access Code : HEX 39/3A/3D/3E A16 Access Code : HEX 29/2D User Defined : HEX 10-17/18-1F
<b>Slave Functions</b>	Dual-ported SRAM for VME; up to 16 software selectable base addresses VME Mailbox IRQ
<b>CXC Interface</b>	DIN 41612(C), 96-pin, 3 NMSI ports, DMA

<sup>1</sup> Available on DM60x Memory Piggyback

<b>VMEbus Interface</b>	DIN 41612(C), 96-pin, P1 connector A24/A16:D16/D8 master and slave
<b>DMA</b>	Two independent channels with 32-bit internal/external transfers
<b>Networking</b>	All Ethernet interfaces conform to IEEE 802-3 and are available on SI-xx piggybacks (only with 68EN360)
<b>Serial-Interfaces</b>	From MC68(EN)360 (ports SMC1 and SMC2) with Standard RS232 configuration
<b>Power Consumption</b>	Typ. 3W for MC68360@ 25 MHz Typ. 3,5W for MC68EN360 @ 33 MHz
<b>Temperature</b>	0°C to +70°C (standard) -40°C to +85°C (extended) -55°C to +85°C (storage)
<b>Humidity</b>	0 to 95% non-condensing
<b>Weight</b>	260 g (with 10BaseT and memory piggybacks)
<b>Dimensions</b>	100 mm x 160 mm 3U format; Single-slot (4HP)
<b>Front Panel Functions</b>	3 LEDs:   red     : Halt yellow : Watchdog enabled green  : General purpose  2 Switches: AB     : Abort function (NMI) RST    : Reset  Other LEDs showing Ethernet or RS485 activity are present depending on the version ordered

**Block scheme of unit**



**Memory Piggyback Options**

## Ordering Information

Product	Description	Order No.
DM 600	Memory Piggyback with 4 MByte DRAM and 4 MByte FLASH memory for VM42/62	11853
DM 602	Memory module with 1 MByte DRAM and 2 MByte FEPRAM for VSBC-32/860 VM42/62/642/662/162/172, IUC-32. Cannot be sold without CPU-BASE-Board.	17556
VSBC-32E-BASE	VMEbus CPU 68EN360 33 MHz, 2*RS232 256 KB DP-SRAM, RTC, CXC Interface, PEPbug. *Memory must be ordered separately, *SI piggyback must be ordered separately.	12480
VSBC-32E-BASE	VMEbus CPU 68EN360 25 MHz, 2*RS232 256 KB DP-SRAM, RTC, CXC Interface, PEPbug. (Ethernet supported) *Memory must be ordered separately, *SI piggyback must be ordered separately.	12897
VSBC-32E-BASE	VMEbus CPU 68360 25 MHz, 2*RS232 256 KB DP-SRAM, RTC, CXC Interface, PEPbug. (No Ethernet supported) *Memory must be ordered separately, *SI piggyback must be ordered separately.	12479
SI-10B2	10Base2 Thin Ethernet interface piggyback with RG58 coax. connector	9925
SI-10BT	Twisted pair (10BaseT) interface for use on the VM42/VM62, VSBC-32 or IUC-32. RJ45 connector cannot be sold without VM42-BASE or VM62-BASE or VSBC32x-BASE or IUC-32x-BASE. Shield connected with GND for CE qual.	15917
SI-10BT-E2	Twisted pair (10BaseT) interface for use on the VM42/VM62, VSBC-32 or IUC-32 in E2. RJ45 connector cannot be sold without VM42-BASE or VM62-BASE or VSBC32x-BASE or IUC-32x-BASE.	15819

**Note :**