

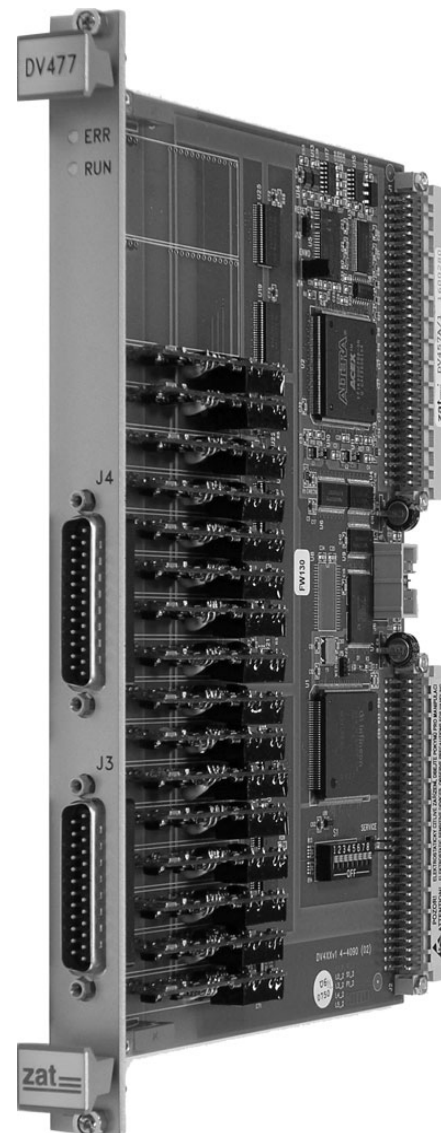
BASIC CHARACTERISTICS

- Connecting 16 analog inputs
- A/D conversion time 83ms
- Input range $\pm 20\text{mA}$, $\pm 5\text{mA}$ DC
- Input resolution 16 bits
- Input accuracy 0,05% per range
- Inputs' galvanic separation off the system and each other
- VME interface

DESCRIPTION

Board DV477 contains sixteen independent galvanic separated input A/D convertors for measurement of DC current signals $\pm 20\text{mA}$ from technological transducers and sensors. The board is used in system ZAT-2000 MP in connection with modules ZAT of series MD, possibly VD, VP, VH a VZ. System interface is formed by VME bus with VME interface A24 (A16):D16. The board is intended for system VME 6HE.

Board DV477 treats input current signals that are converted to digital form with 24-bit resolution, from which 16 bits (15 bits and sign) are used for next processing. Programming could increase each input sensitivity 4 times (from $\pm 20\text{mA}$ to $\pm 5\text{mA}$). Digital communication with control board is done through VME bus. The board does not utilize VME bus interruption system. After passage through input filter, analog signal of each input is converted into digital data by separate Σ - Δ A/D convertor. After the conversion signals are led through galvanic separation by means of optocouplers into internal bus and subsequently processed by controller. CPU controls processing of analog signals and their digital filtering.



DV477 could be adjusted in specialized workplace and resulting calibration constants are stored in the board's Flash memory.

MEMORY MAP

Detailed description of memory map is included in document „Board DV477, Service manual“, id. 07039.

- BIR – *Board Identification Register*
board identification no. – AA57H
- NAR – Address Register
Board BASE ADR in access
A23 (i.e. address A23-A8).
- OIW – Output Input Width
Input and output field length
00E0h
- DRW – Diagnostic and DPRAM field
length - 0020h
- SAW – Control and Status Register
length 0000h
- CR – Control Register
- SR – Status Register

Board's base address of A16 access is set through switch S1 by blocks of 64 byte. Block address of A24 access is set by SW driver at board's initialization through record into NAR register.

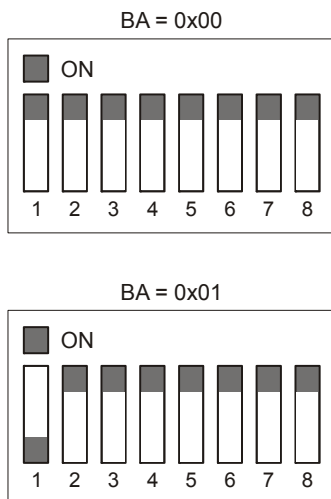


Fig.1 Base address switch

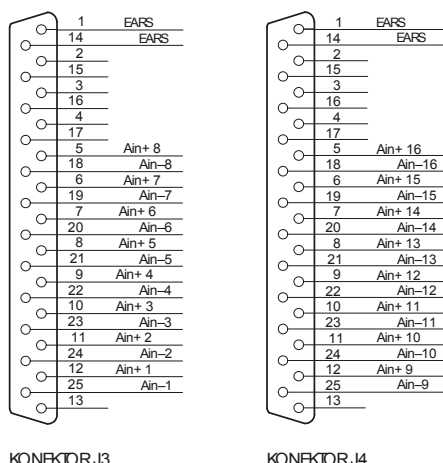


Fig.2 Board DV477 connector pinout

INDIVIDUAL CIRCUITS DESCRIPTION

Heart of connection is created by processor with cycle frequency 25MHz, which controls all the board functions. After feeding connection or signal RESET activation the processor performs test of entire board's hardware and system's integrity test. Red LED ERR lights on board's front panel. Yellow LED RUN starts flashing (with period approx. 1s) after successful board's hardware test. Yellow LED RUN flashes with period approx. 330ms (three times faster) if the board is switched to mode for adjusting. Till after board's software initialization and its accepting by CPU program red LED ERR lights off and yellow LED RUN lights permanently. Yellow LED RUN lights permanently at proper board operation.

Current signal ±20mA (±5mA) is led to sensing resistors of board's analog inputs. Each measuring channel is equipped with analog low filter with protection circuit against pulse overvoltage, which reduces input frequencies higher than 2kHz.

Analog current signal is sensed in precise resistor with value 50Ω by separate Σ-Δ A/D convertor with digital filter of system frequency 50Hz. Itself convertor has resolution 24 bits, from which processor's FW selects valid part for transfer to the system by selected range. A/D convertor's self/calibration is done in each conversion

cycle. Converter's conversion time is 80ms, where 40ms are reserved for input signal's sampling. This feature enables to reach high interference suppression in system frequencies. Measurement in all the input channels is synchronous and cyclic one. Individual input channels could be SW adjusted to amplification 1 (range I) or 4 (range II). Input voltage limits' exceeding and input module's fatal error are indicated in diagnostic report for each channel. Concerning design, each input's analog circuits forms separate module, on

which protection circuits, itself A/D converter, reference feeder, galvanic separation circuits and DC/DC converter for circuit feeding are placed. Each module input is connected through capacitance 10nF to EARS bus and this bus is connected through capacitance 0,2μF to board chassis (panel). Concerning test purposes, EARS bus is led to connectors J3 and J4. These pins are not connected in standard ZAT cabling.

TECHNICAL PARAMETERS

Parameter	Conditions	Min.	Type	Max.	Units
Feeding voltage (VME)		+4,75 +11,4 -11,4	+5 +12 -12	+5,25 +12,8 -12,8	V
Consumption	+5V +12V -12V		170 65 -	190 80 -	mA
Board power				1,9	W
Dielectric strength	input/system, 1 min.	1050			V DC
Dielectric strength	input/input, 1 min	720			V DC
Insulation resistance	against board panel	20			MΩ
Input range I Input range II	SW programmable		±20 ±5		mA
Range overrun	at measurement range			±20	%
Range overrun	without input circuits' damage			±50	mA
A/D conversion time			83		ms
Input accuracy after calibr. at ambient temp. 23±2°C	range I range II		0,02 0,02	0,05 0,05	%
Input accuracy without calibr. at ambient temp. 23±2°C			0,06	0,1	%
Integral non-linearity at ambient temp. 23±2°C	range I, II		0,005	0,01	%
Additional input errors (data error caused by change of)	ambient temperature feeding voltage ±12V		0,001	0,002 0,001	% / K % / V
Input resistance			86		Ω
Signal 50Hz suppression		100	110		dB
Operational temperature range		-5		+70	°C
Humidity (non-condensing)		5		95	%
Storing temperature		-20		+85	°C
Connector	IN 1÷16	D-Sub, 25 pin			

Parameter	Conditions	Min.	Type	Max.	Units
Weight			400		g
Dimension			6HE, 4TE		

DV477 INPUT VALUE TABLE

Input value	Output value	Range overrun	±20 mA	±5 mA
$\geq I_{HLI} = 1,25 * I_{RNG}$	7FFF /HEX/	1	$\geq +25,000 \text{ mA}$	$\geq +6,250 \text{ mA}$
$I_{MAX} (1,25 * I_{RNG} - 1 \text{ LSB})$	7FFF /HEX/	0	$\sim +24,99924 \text{ mA}$	$\sim +6,24981 \text{ mA}$
$+ I_{RNG}$	6666 /HEX/	0	20,000 mA	5,000 mA
0	0000 /HEX/	0	0,000 mA	0,000 mA
- 1LSB	FFFF /HEX/	0	$\sim -0,00076 \text{ mA}$	$\sim -0,00019 \text{ mA}$
$- I_{RNG}$	9999 /HEX/	0	- 20,000 mA	- 5,000 mA
$I_{MIN} (- 1,25 * I_{RNG})$	8000 /HEX/	0	- 25,000 mA	- 6,250 mA
$< I_{LLI} = - 1,25 * I_{RNG}$	8000 /HEX/	1	$< - 25,000 \text{ mA}$	$< - 6,250 \text{ mA}$

1 LSB $\approx 0,763 \mu\text{A}$ ($\approx 0,019 \mu\text{A}$)

Table accuracy is guaranteed in value range $- I_{RNG} .. +I_{RNG}$ (see Technical parameters). Input linearity is guaranteed in value range $I_{MIN} .. I_{MAX}$ (see Technical parameters). Values I_{HLI} and I_{LLI} are limit ones, when convertor range overrun is not reported yet.

DV477 DESIGN TABLE

Order identification	Count		Function		Note
	inputs	outputs	input	output	
DV477	16	-	±20mA ±5mA	-	input module CA005

BLOKOVÉ SCHÉMA ZAPOJENÍ DESKY DV477

